Matoshri College of Engineering and Research Center Nasik
Department of Computer Engineering

Digital Elecronics and Logic Design (DELD)
UNIT - III

Class : S.E.Comp **Subject : DELD**

Sr. No.	Question	Option A	Option B	Option C	Option D	Correct Option	Marks
1	In the following question, match each of the items A, B and C on the left with an approximation item on the right A. Shift register can be used 1. for code conversion B. A multiplexer can be used 2. to generate memory slipto select C. A decoder can be used 3. for parallel to serial conversion 4. as many to one switch 5. for analog to digital conversion	A B C 1 2 3	A B C 3 4 1	A B C 5 4 2	A B C 1 3 5	**B**	**4**
2	A standard SOP form has _____ terms that have all the variables in the domain of the expression.	SUM	SUB	Mult	DIV	**A**	**1**
3	How many data select lines are required for selecting eight inputs?	1	2	3	4	**C**	**2**
4	Half adder circuit is ____?	Half of an AND gate	A circuit to add two bits together	Half of a NAND gate	none of above	**B**	**2**
5	The full adder adds the Kth bits of two numbers to the	difference of the previous bits	sum of all previous bits	carry from (K - 1)TH bit	sum of previous bit	**C**	**2**
6	The number of two input multiplexers required to construct a 210 input multiplexer is,	31	10	127	1023	**D**	**2**
7	A small dot or circle printed on top of an IC indicates	Vcc	Gnd	Pin 14	Pin 1	**D**	**1**

8	Which of the following adders can add three or more numbers at a time ?	Parallel adder	Carry-look-ahead adder	Carry-save-adder D.	Full adder	**B**	**2**
9	An AND circuit	is a memory circuit	gives an output when all input signals are present simultaneously	is a -ve OR gate	is a linear circuit	**B**	**2**
10	What are the three output conditions of a three-state buffer?	HIGH, LOW, float	1, 0, float	both of the above	neither of the above	**C**	**2**
11	When is it important to use a three-state buffer?	when two or more outputs are connected to the same input	when all outputs are normally HIGH	when all outputs are normally LOW	when two or more outputs are connected to two or more inputs	**A**	**2**
12	The device which changes from serial data to parallel data is	COUNTER	MULTIPLEXER	DEMULTIPLEXER	FLIP-FLOP	**C**	**2**
13	A device which converts BCD to Seven Segment is called	MULTIPLEXER	DEMULTIPLEXER	ENCODER	DECODER	**D**	**2**
14	How many 3-line-to-8-line decoders are required for a 1-of-32 decoder?	1	2	4	8	**C**	**2**
15	A device which converts BCD to Seven Segment is called	Encoder	Decoder	Multiplexer	Demultiplexer	**B**	**2**
16	A multiplexer is a logic circuit that	accepts one input and gives several output	accepts many inputs and gives many output	accepts many inputs and gives one output	accepts one input and gives one output	**C**	**2**

17	In order to implement a n variable switching function, a MUX must have	2n inputs	2n+1 inputs	2n-1 inputs	2n-1 inputs	**A**	**2**
18	Logic gates with a set of input and outputs is arrangement of	Combinational circuit	Logic circuit	Design circuits	Register	**A**	**2**
19	A latch is constructed using two cross-coupled	AND and OR gates	AND gates	NAND and NOR gates	NAND gates	**D**	**2**
20	A combinational logic circuit which sends data coming from a single source to two or more separate destinations is	Decoder	Encoder	Multiplexer	Demultiplexer	**D**	**2**
21	Data can be changed from special code to temporal code by using	Shift registers	Counters	Combinational circuits	A/D converters	**A**	**2**
22	A device which converts BCD to Seven Segment is called	Encoder	Decoder	Multiplexer	Demultiplexer		
23	The gray code equivalent of (1011)2 is	1101	1010	1110	1111	**B**	**2**
24	Odd parity of word can beconveniently tested by	OR gate	AND gate	NOR gate	XOR gate	**D**	**2**
25	Which one of the following will give the sum of full adders as output ?	Three point majority circuit	Three bit parity checker	Three bit comparator	Three bit counter	**D**	**2**
26	The number of full and half-adders required to add 16-bit numbers is	8 half-adders, 8 full-adders	1 half-adder, 15 full-adders	16 half-adders, 0 full-adders	4 half-adders, 12 full-adders	**B**	**2**
27	A one-to-four line demultiplexer is to be implemented using a memory. How many bits must each word have ?	1 bit	2 bits	4 bits	8 bits	**A**	**2**

28	What logic function is produced by adding an inverter to the output of an AND gate ?	NAND	NOR	XOR	OR	**A**	**1**
29	A demultiplexer is used to	Route the data from single input to one of many outputs	Select data from several inputs and route it to single output	Perform serial to parallel conversion	All of these	**A**	**1**
30	How many full adders are required to construct an m-bit parallel adder ?	m/2	m-1	m	m+1	**B**	**1**
31	Parallel adders are	combinational logic circuits	sequential logic circuits	both (a) and (b)	None of these	**B**	**1**
32	The digital multiplexer is basically a combination logic circuit to perform the operation	AND-AND	OR-OR	AND-OR	OR-AND	**C**	**2**
33	How many lines the truth table for a four-input NOR gate would contain to cover all possible input combinations ?	4	8	12	16	**D**	**2**
34	How many truth tables can be made from one function table ?	1	2	3	ANY NO	**B**	**2**

35	A comparison between serial and parallel adder reveals that serial order	is slower	is faster	operates at the same speed as parallel adder	is more complicated	**A**	**2**
36	What is the largest number of data inputs which a data selector with two control inputs can have ?	2	4	6	8	**B**	**1**
37	If a logic gates has four inputs, then total number of possible input combinations is	4	8	16	32	**C**	**1**
38	If a logic gates has four inputs, then total number of possible input combinations is	input combination at the time	input combination and the previous output	nput combination at that time and the previous input combination	present output and the previous output	**A**	**2**
39	A combinational logic circuit which generates a particular binary word or number is	Decoder	Multiplexer	Encoder	Demultiplexer	**A**	**1**
40	Which of the following circuit can be used as parallel to serial converter ?	Multiplexer	Demultiplexer	Decoder	Digital counter	**A**	**2**

41	In which of the following adder circuits, the carry look ripple delay is eliminated ?	Half adder	Full adder	Parallel adder	Carry-look-ahead adder	**C**	**2**
42	Adders	adds 2 bits	is called so because a full adder involves two half-adders	needs two input and generates two output	All of these	**D**	**2**
43	Excess-3 code is known as	Weighted code	Cyclic redundancy code	Self-complementing code	Algebraic code.	**C**	**1**
44	The number of control lines for 32 to 1 multiplexer is	4	16	5	6	**C**	**2**
45	The selector inputs to an arithmetic-logic unit (ALU) determine the:	selection of	arithmetic	data word	clock	**B**	**2**
46	What are the two types of basic adder circuits?	half adder and	half adder	asynchronou	one's	**A**	**2**
47	The inverter OR-gate and AND gate are called deeision-making elements because they can recognize some input while disregarding others. A gate	words,high	bytes,low	bytes,high	character,low	**A**	**2**
48	Which one of the following set of gates are best suited for 'parity' checking and 'parity' generation.	AND, OR, NOT gates	EX-NOR or EX-OR gates	NAND gates	NOR gates	**B**	**2**
49	What are the three output conditions of a three-state buffer?	HIGH, LOW, float	1, 0, float	both of the above	neither of the above	**C**	**2**

50	When is it important to use a three-state buffer?	when two or more outputs are connected to the same input	when all outputs are normally HIGH	when all outputs are normally LOW	when two or more outputs are connected to two or more inputs	**A**	**2**
51	How many inputs are required for a 1-of-10 BCD decoder?	4	8	10	1	**A**	1
52	Most demultiplexers facilitate which of the following?	decimal to hexadecimal	single input, multiple outputs	ac to dc	odd parity to even parity	**B**	1
53	One application of a digital multiplexer is to facilitate:	code conversion	parity checking	parallel-to-serial data conversion	data generation	**C**	1
54	Select one of the following statements that best describes the parity method of error detection:	best suited for detecting single-bit errors in transmitted codes.	best suited for detecting double-bit errors that occur during the transmission of codes from one location to another.	A AND B	NONE OF THE ABOVE	**A**	2
55	A multiplexed display:	accepts data inputs from one line and passes this data to multiple output lines	uses one display to present two or more pieces of information	accepts data inputs from multiple lines and passes this data to multiple output lines	accepts data inputs from several lines and multiplexes this input data to four BCD lines	**B**	1

56	In which of the following gates, the output is 1, if and only if at least one input is 1?	NOR	AND	OR	NAND	**C**	1
57	The time required for a gate or inverter to change its state is called	Rise time	Decay time	Propagation time	Charging time	**C**	1
58	The time required for a pulse to change from 10 to 90 percent of its maximum value is called	Rise time	Decay time	Propagation time	Operating speed	**A**	1
59	The maximum frequency at which digital data can be applied to gate is called	Operating speed	Propagation speed	Binary level transaction period	Charging time	**A**	1
60	What is the minimum number of two-input NAND gates used to perform the function of two input OR gate ?	one	two	three	Four	**C**	2
61	Odd parity of word can beconveniently tested by	OR gate	AND gate	NOR gate	XOR gate	**D**	1
62	Which one of the following will give the sum of full adders as output ?	Three point majority circuit	Three bit parity checker	Three bit comparator	Three bit counter	**D**	1
63	The number of full and half-adders required to add 16-bit numbers is	8 half-adders, 8 full-adders	1 half-adder, 15 full-adders	16 half-adders, 0 full-adders	4 half-adders, 12 full-adders	**B**	1
64	The time required for a pulse to decrease from 90 to 10 per cent of its maximum value is called	Rise time	Decay time	Binary level transition period	Propagation delay	**B**	1
65	Which of the following gates would output 1 when one input is 1 and other input is 0 ?	OR gate	AND gate	NAND gate	AND gate	**D**	1
66	Which of the following statements is wrong ?	Propagation delay is the time required for a gate to change its state	Noise immunity is the amount of noise which can be applied to the input of a gate without causing the gate to change state	Fan-in of a gate is always equal to fan-out of the same gate	Operating speed is the maximum frequency at which digital data can be applied to a gate	**C**	1

67	Which of the following expressions is not equivalent to X ' ?	X NAND X	X NOR X	X NAND 1	X NOR 1	**D**	1
68	Which of the following gates are added to the inputs of the OR gate to convert it to the NAND gate ?	NOT	AND	OR	XOR	**A**	1
69	The EXCLUSIVE NOR gate is equivalent to which gate followed by an inverter ?	OR gate	AND	NAND	XOR	D	1
70	A one-to-four line demultiplexer is to be implemented using a memory. How many bits must each word have ?	1 BIT	2 BITS	4 BITS	8 BITS	A	1
71	What logic function is produced by adding an inverter to the output of an AND gate ?	NAND	NOR	XOR	OR	A	1
72	Which of the following gates is known as coincidence detector ?	AND GATE	OR GATE	NOT GATE	NAND GATE	A	1
73	Which table shows the logical state of a digital circuit output for every possible combination of logical states in the inputs ?	Function table	Truth table	Routing table	ASCII table	B	1
74	A positive AND gate is also a negative	NAND gate	NOR gate	AND GATE	OR GATE	D	1
75	A demultiplexer is used to	Route the data from single input to one of many outputs	Select data from several inputs and route it to single output	Perform serial to parallel conversion	All of these	A	1
76	An OR gate can be imagined as	Switches connected in series	Switches connected in parallel	MOS transistors connected in series	None of these	B	1
77	Which combination of gates does not allow the implementation of an arbitrary boolean function?	OR gates and AND gates only	OR gates and exclusive OR gate only	OR gates and NOT gates only	NAND gates only	A	1
78	How many full adders are required to construct an m-bit parallel adder ?	m/2	m-1	m	m+1	B	2
79	Parallel adders are	combinational logic circuits	sequential logic circuits	both (a) and (b)	None of these	A	1

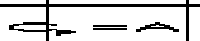
80	The digital multiplexer is basically a combination logic circuit to perform the operation	AND-AND	OR-OR	AND-OR	OR-AND	C	1
81	The output of NOR gate is	High if all of its inputs are high	Low if all of its inputs are low	High if all of its inputs are low	High if only of its inputs is low	C	1
82	How many lines the truth table for a four-input NOR gate would contain to cover all possible input combinations ?	4	8	12	16	D	1
83	A toggle operation cannot be performed using a single	NOR gate	AND gate	NAND gate	XOR gate	B	1
84	Which table shows the electrical state of a digital circuit's output for every possible combination of electrical states in the inputs ?	Function table	Truth table	Routing table	ASCII table	A	1
85	What is the minimum number of 2 input NAND gates required to implement the function F = (x'+y') (z+w)	6	5	4	3	C	1
86	How many truth tables can be made from one function table ?	One	Two	Three	Any numbers	B	1
87	A comparison between serial and parallel adder reveals that serial order	is slower	is faster	operates at the same speed as parallel adder	is more complicated	A	1
88	What is the largest number of data inputs which a data selector with two control inputs can have ?	2	4	8	16	B	1
89	If a logic gates has four inputs, then total number of possible input combinations is	4	8	16	32	C	1
90	A combinational circuit is one in which the output depends on the	input combination at the time	input combination and the previous output	input combination at that time and the previous input combination	present output and the previous output	A	1

91	The function of a multiplexer is	to decode information	to select 1 out of N input data sources and to transmit it to single channel	to transit data on N lines	to perform serial to parallel conversion	B	1
92	A combinational logic circuit which generates a particular binary word or number is	Decoder	Multiplexer	Encoder	Demultiplexer	A	1
93	Which of the following circuit can be used as parallel to serial converter ?	Multiplexer	Demultiplexer	Decoder	Digital counter	A	1
94	In which of the following adder circuits, the carry look ripple delay is eliminated ?	Half adder	Full adder	Parallel adder	Carry-look-ahead adder	C	1
95	Adders	adds 2 bits	Is called so because a full adder involves two half-adders	needs two input and generates two output	All of these	A	1
96	How many 3-line-to-8-line decoders are required for a 1-of-32 decoder?	1	2	4	8	C	1
97	For the device shown here, let all D inputs be LOW, both S inputs be HIGH, and the input be LOW. What is the status of the Y output?	LOW	HIGH	Don't Care	Cannot be determined	A	1
98	Convert BCD 0001 0010 0110 to binary.	1111110	1111000	1111101	1111111	A	2
99	Convert BCD 0001 0111 to binary.	10101	10001	10010	11000	C	2
100	How many data select lines are required for selecting eight inputs?	1	2	3	4	C	1
101	How many 1-of-16 decoders are required for decoding a 7-bit binary number?	5	6	7	8	D	1
102	The implementation of simplified sum-of-products expressions may be easily implemented into actual logic circuits using all universal _____ gates with little or no increase in circuit complexity. (Select the response for the blank space that will BEST make the statement true.)	AND/OR	NAND	NOR	OR/AND	B	1

103	Which of the following statements accurately represents the two BEST methods of logic circuit simplification?	Boolean algebra and Karnaugh mapping	Karnaugh mapping and circuit waveform analysis	Actual circuit trial and error evaluation and waveform analysis	Boolean algebra and actual circuit trial and error evaluation	A	1
104	Which of the following combinations cannot be combined into K-map groups?	Corners in the same row	Corners in the same column	Diagonal corners	Overlapping combinations	C	2
105	As a technician you are confronted with a TTL circuit board containing dozens of IC chips. You have taken several readings at numerous IC chips, but the readings are inconclusive because of their erratic nature. Of the possible faults listed, select the one that most probably is causing the problem.	A defective IC chip that is drawing excessive current from the power supply	A solar bridge between the inputs on the first IC chip on the board	An open input on the first IC chip on the board	A defective output IC chip that has an internal open to V_{cc}	C	2
106	Which gate is best used as a basic comparator?	NOR	OR	Exclusive-OR	AND	C	1
107	The device shown here is most likely a _____.	comparator	multiplexer	demultiplexer	parity generator	C	2
108	For the device shown here, assume the D input is LOW, both S inputs are HIGH, and the input is HIGH. What is the status of the outputs?	All are HIGH.	All are LOW.	All but are LOW.	All but are HIGH.	A	1
109	In VHDL, macrofunctions is/are:	digital circuits.	analog circuits.	a set of bit vectors.	preprogrammed TTL devices.	D	1
110	Which of the following expressions is in the product-of-sums form?	$(A + B)(C + D)$	$(AB)(CD)$	$AB(CD)$	$AB + CD$	A	2

111	Which of the following is an important feature of the sum-of-products form of expressions?	All logic circuits are reduced to nothing more than simple AND and OR operations.	The delay times are greatly reduced over other forms.	No signal must pass through more than two gates, not including inverters.	The maximum number of gates that any signal must pass through is reduced by a factor of two.	A	1
112	An output gate is connected to four input gates; the circuit does not function. Preliminary tests with the DMM indicate that the power is applied; scope tests show that the primary input gate has a pulsing signal, while the interconnecting node has no signal. The four load gates are all on different ICs. Which instrument will best help isolate the problem?	Current tracer	Logic probe	Oscilloscope	Logic analyzer	A	1
113	The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?	A > B = 1, A < B = 0, A < B = 1	A > B = 0, A < B = 1, A = B = 0	A > B = 1, A < B = 0, A = B = 0	A > B = 0, A < B = 1, A = B = 1	C	4
114	A logic probe is placed on the output of a gate and the display indicator is dim. A pulser is used on each of the input terminals, but the output indication does not change. What is wrong?	The output of the gate appears to be open.	The dim indication on the logic probe indicates that the supply voltage is probably low.	The dim indication is a result of a bad ground connection on the logic probe.	The gate may be a tristate device.	A	1

115	Each "1" entry in a K-map square represents:	a HIGH for each input truth table condition that produces a HIGH output.	a HIGH output on the truth table for all LOW input combinations.	a LOW output for all possible HIGH input conditions.	a DON'T CARE condition for all possible input truth table combinations.	A	1
116	Looping on a K-map always results in the elimination of:	variables within the loop that appear only in their complemented form.	variables that remain unchanged within the loop.	variables within the loop that appear in both complemented and uncomplemented form.	variables within the loop that appear only in their uncomplemented form.	C	2
117	What will a design engineer do after he/she is satisfied that the design will work?	Put it in a flow chart	Program a chip and test it	Give the design to a technician to verify the design	Perform a vector test	B	2
118	What is the indication of a short on the input of a load gate?	Only the output of the defective gate is affected.	There is a signal loss to all gates on the node.	The affected node will be stuck in the LOW state.	There is a signal loss to all gates on the node, and the affected node will be stuck in the LOW state.	D	1

119	In HDL, LITERALS is/are:	digital systems.	scalars.	binary coded decimals.	a numbering system.	B	1
120	Which of the following expressions is in the sum-of-products form?	$(A + B)(C + D)$	$(AB)(CD)$	$AB(CD)$	$AB + CD$	D	1
121	The carry propagation can be expressed as _____.	$C_p = AB$	$C_p = A + B$			B	1
122	A decoder can be used as a demultiplexer by _____.	tying all enable pins LOW	tying all data-select lines LOW	tying all data-select lines HIGH	using the input lines for data selection and an enable line for data input	D	1
123	How many 4-bit parallel adders would be required to add two binary numbers each representing decimal numbers up through 300_{10}?	1	2	3	4	C	1
124	Which statement below best describes a Karnaugh map?	A Karnaugh map can be used to replace Boolean rules.	The Karnaugh map eliminates the need for using NAND and NOR gates.	Variable complements can be eliminated by using Karnaugh maps.	Karnaugh maps provide a visual approach to simplifying Boolean expressions.	D	1
125	A certain BCD-to-decimal decoder has active-HIGH inputs and active-LOW outputs. Which output goes LOW when the inputs are 1001?	0	3	9	None. All outputs are HIGH.	C	1
126	A full-adder has a $C_{in} = 0$. What are the sum and the carry (Cout) when A = 1 and B = 1?	= 0, $C_{out} = 0$	= 0, C_{out} = 1	= 1, C_{out} = 0	= 1, $C_{out} = 1$	B	1
127	When adding an even parity bit to the code 110010, the result is _____.	1110010	110010	1111001	1101	A	1
128	Which of the following combinations of logic gates can decode binary 1101?	One 4-input AND gate	One 4-input AND gate, one OR gate	One 4-input NAND gate, one inverter	One 4-input AND gate, one inverter	D	1

129	What is the indication of a short to ground in the output of a driving gate?	Only the output of the defective gate is affected.	There is a signal loss to all load gates.	The node may be stuck in either the HIGH or the LOW state.	The affected node will be stuck in the HIGH state.	B	1
130	How many outputs would two 8-line-to-3-line encoders, expanded to a 16-line-to-4-line encoder, have?	3	4	5	6	B	1
131	A half-adder does not have _____.	carry in	carry out	two inputs	all of the above	A	1
132	_____ is a correct combination for an ODD-parity data transmission system.	data = 1101 1011 parity = 1	data = 1101 0010 parity = 0	data = 0001 0101 parity = 1	data = 1010 1111 parity = 0	A	1
133	A circuit that can convert one of ten numerical keys pressed on a keyboard to BCD is a _____.	priority encoder	decoder	multiplexer	demultiplexer	A	1
134	The _____ prefix on IC's indicates a broader operating temperature range, and the devices are generally used by the military.	54	2N	74	TTL	A	1
135	When an open occurs on the input of a TTL device, the output will _____.	go LOW, because there is no current in an open circuit	react as if the open input were a HIGH	go HIGH, since full voltage appears across an open	still be good, if only the good inputs are used	B	1
136	The largest truth table that can be implemented directly with an 8-line-to-1-line MUX has _____.	3 rows	4 rows	8 rows	16 rows	C	1
137	Parity generation and checking is used to detect _____.	which of two numbers is greater	errors in binary data transmission	errors in arithmetic in computers	when a binary counter counts incorrectly	B	1
138	Except for _____, STD_LOGIC may have the following values.	'z'	'U'	'?'	'L'	C	1
139	A gate that could be used to compare two logic levels and provide a HIGH output if they are equal is a(n) _____.	XOR gate	XNOR gate	NAND gate	NOR gate	B	1

140	VHDL is very strict in the way it allows us to assign and compare _____ such as signals, variables, constants, and literals.	objects	LOGIC_VECTORS	designs	arrays	A	1
141	The AND-OR-INVERT gates are designed to simplify implementation of _____.	POS logic	DeMorgan's theorem	NAND logic	SOP logic	B	1
142	The output of a gate has an internal short; a current tracer will _____.	identify the defective gate	show whether the gate is shorted to V_{cc} or ground	probably not be able to locate the problem	be able to identify the defective load node	A	1
143	Parity generators and checkers use _____ gates.	exclusive-AND	exclusive-OR/NOR	exclusive-OR	exclusive-NAND	B	1
144	The 7447A is a BCD-to-7-segment decoder with ripple blanking input and output functions. The purpose of these lines is to _____.	turn off the display for any nonsignificant digit	turn off the display for any zero	turn off the display for leading or trailing zeros	test the display to assure all segments are operational	A	1
145	One reason for using the sum-of-products form is that it can be implemented using all _____ gates without much difficulty.	NOR	NAND	AND	DOOR	B	1
146	When an open occurs on the input of a CMOS gate, the output will _____.	go LOW, because there is no current in an open circuit	react as if the open input were a HIGH	go HIGH, since full voltage appears across an open	be unpredictable; it may go HIGH or LOW	D	2
147	To subtract a signed number (the subtrahend) from another signed number (the minuend) in the 2's complement system, the minuend is _____.	complemented only if it is positive	complemented only if it is negative	always complemented	never complemented	D	2
148	In an odd-parity system, the data that will produce a parity bit = 1 is _____.	data = 1010011	data = 1111000	data = 1100000	All of the above	D	2
149	The addition of two signed numbers in the 2's complement system can cause overflow. For overflow to occur both numbers must _____.	be positive	be negative	have the same sign	have opposite signs	C	2

150	A Karnaugh map will _____.	eliminate the need for tedious Boolean simplifications	allow any circuit to be implemented with just AND and OR gates	produce the simplest sum-of-products expression	give an overall picture of how the signals flow through the logic circuit	A	2
151	An 8-bit binary number is input to an odd parity generator. The parity bit will equal 1 only if _____.	the number is odd	the number of 1s in the number is odd	the number is even	the number of 1s in the number is even	D	2
152	Two 4-bit comparators are cascaded to form an 8-bit comparator. The cascading inputs of the most significant 4 bits should be connected _____.	to the outputs from the least significant 4-bit comparator	to the cascading inputs of the least significant 4-bit comparator	A = B to a logic high, A < b and a > B to a logic low	ground	A	1
153	When Karnaugh mapping, we must be sure to use the _____ number of loops.	maximum	minimum	median	Karnaugh	B	1
154	The final output of a POS circuit is generated by _____.	an AND	an OR	a NOR	a NAND	A	2
155	After each circuit in a subsection of a VHDL program has been _____, they can be combined and the subsection can be tested.	designed	tested	engineered	produced	B	1
156	The _____ series of IC's are pin, function, and voltage-level compatible with the 74 series IC's.	ALS	CMOS	HCT	2N	C	2
157	The _____ circuit produces a HIGH output whenever the two inputs are equal.	exclusive-AND	exclusive-NAND	exclusive-NOR	exclusive-OR	C	2
158	A 4-bit adder has the following inputs: $C_0 = 0$, $A_1 = 0$, $A_2 = 1$, $A_3 = 0$, $A_4 = 1$, $B_1 = 0$, $B_2 = 1$, $B_3 = 1$, $B_4 = 1$. The output will be _____.	1100	10101	11000	11	C	2
159	The _____ statement evaluates the variable status.	IF/THEN	IF/THEN/ELSE	CASE	ELSIF	A	2
160	In VHDL, data can be each of the following types except _____.	BIT	BIT_VECTOR	STD_LOGIC	STD_VECTOR	D	2
161	When grouping cells within a K-map, the cells must be combined in groups of _____.	2's	1, 2, 4, 8, etc.	4's	3's	B	1

162	The _____ circuit produces a HIGH output whenever the two inputs are unequal.	exclusive-AND	exclusive-NOR	exclusive-OR	inexclusive-OR	C	1
163	Occasionally, a particular logic expression will be of no consequence in the operation of a circuit, such as in a BCD-to-decimal converter. These result in _____ terms in the K-map and can be treated as either _____ or _____, in order to _____ the resulting term.	don't care, 1's, 0's, simplify	spurious, AND's, OR's, eliminate	duplicate, 1's, 0's, verify	spurious, 1's, 0's, simplify	A	2
164	A good rule of thumb for determining the pin numbers of dual-in-line package IC chips would be to place the notch to your right and pin #1 will always be in the lower right corner.	TRUE	FALSE	None of the above	Can not predict	B	2
165	The carry output of each adder in a ripple adder provides an additional sum output bit.	TRUE	FALSE	None of the above	Can not predict	A	1
166	Truth tables are great for listing all possible combinations of independent variables.	TRUE	FALSE	None of the above	Can not predict	A	1
167	A square in the top row of a K-map is considered to be adjacent to its corresponding square in the bottom row.	TRUE	FALSE	None of the above	Can not predict	A	1
168	To implement the full-adder sum functions, two exclusive-OR gates can be used.	TRUE	FALSE	None of the above	Can not predict	A	1
169	The input at the 1, 2, 4, 8 inputs to a 4-line to 16-line decoder with active-low outputs is 1110. As a result, output line 7 is driven LOW.	TRUE	FALSE	None of the above	Can not predict	B	2
170	When decisions demand two possible actions, the IF/THEN/ELSE control structure is used.	TRUE	FALSE	None of the above	Can not predict	A	2
171	TTL stands for transistor-technology-logic.	TRUE	FALSE	None of the above	Can not predict	B	1
172	The 54 prefix on ICs indicates a broader operating temperature range, generally intended for military use.	TRUE	FALSE	None of the above	Can not predict	A	2
173	This is an example of a POS expression:	TRUE	FALSE	None of the above	Can not predict	A	2
174	The abbreviation for an exclusive-OR gate is XOR.	TRUE	FALSE	None of the above	Can not predict	A	2
175	In an even-parity system, the parity bit is adjusted to make an even number of one bits.	TRUE	FALSE	None of the above	Can not predict	A	2
176	In an even-parity system, the following data will produce a parity bit = 1. data = 1010011	TRUE	FALSE	None of the above	Can not predict	B	2
177	The following combination is correct for an ODD parity data transmission system: data = 011011100 and parity = 0	TRUE	FALSE	None of the above	Can not predict	A	1
178	The XOR gate will produce a HIGH output if only one but not both of the inputs is HIGH.	TRUE	FALSE	None of the above	Can not predict	A	1

179	When decisions demand one of many possible actions, the ELSIF control structure is used.	TRUE	FALSE	None of the above	Can not predict	A	1
180	The K-map provides a "graphical" approach to simplifying sum-of-products expressions.	TRUE	FALSE	None of the above	Can not predict	A	1
181	Even parity is the condition of having an even number of 1s in every group of bits.	TRUE	FALSE	None of the above	Can not predict	A	1
182	The look-ahead carry method suffers from propagation delays.	TRUE	FALSE	None of the above	Can not predict	B	1
183	A pull-up resistor is a resistor used to keep a given point in a circuit HIGH when in the active state.	TRUE	FALSE	None of the above	Can not predict	A	1
184	A data selector is also called a demultiplexer.	TRUE	FALSE	None of the above	Can not predict	B	1
185	A digital circuit that converts coded information into a familiar or non-coded form is known as an encoder.	TRUE	FALSE	None of the above	Can not predict	B	1
186	An exclusive-OR gate will invert a signal on one input if the other is always HIGH.	TRUE	FALSE	None of the above	Can not predict	A	1
187	The following combination is correct for an EVEN parity data transmission system: data = 100111100 and parity = 0	TRUE	FALSE	None of the above	Can not predict	B	2
188	The CASE control structure is used when an expression has a list of possible values.	TRUE	FALSE	None of the above	Can not predict	A	2
189	An encoder in which the highest and lowest value input digits are encoded simultaneously is known as a priority encoder.	TRUE	FALSE	None of the above	Can not predict	B	2
190	Three select lines are required to address four data input lines.	TRUE	FALSE	None of the above	Can not predict	B	2
191	Single looping in groups of three is a common K-map simplification technique.	TRUE	FALSE	None of the above	Can not predict	B	2
192	In true sum-of-products expressions, the inversion signs cannot cover more than single variables in a term.	TRUE	FALSE	None of the above	Can not predict	A	2
193	A combinatorial logic circuit has memory characteristics that "remember" the inputs after they have been removed.	TRUE	FALSE	None of the above	Can not predict	B	2